REMARKS

Claims 1-16, 21-22 and 24-25 are pending. By this amendment, claims 1, 9 and 16 are amended and claims 24-25 are added. Support for the amendments to claims 1 and 16 and new claims 24-25 can be found on page 10, lines 9-16 and page 11, lines 12-16. No new matter has been added. Applicants respectfully request reconsideration and timely withdrawal of the pending objections and rejections for the reasons discussed below.

35 U.S.C. §102(e) Rejection

Claims 1, 2 and 16 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No.: 6,573,172 to EN, *et al.* ("EN"). This rejection is respectfully traversed.

In order to establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must disclose each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that a *prima facie* case of anticipation cannot be established because SAUNDERS fails to teach each and every element of the claims.

More particularly, amended independent claim 1 recites, *inter alia,*

> removing, after the oxidizing step, oxide above the gate polysilicon of the n-type transistor, wherein the oxidizing step results in formation of a bird's beak in an edge of the gate polysilicon.

Additionally, amended independent claim 16 recites, *inter alia,*

> removing oxide above the gate polysilicon of the n-type transistor, wherein the oxidizing step results in formation of a bird's beak within the channel of the n-type transistor in an edge of the gate polysilicon.

Applicants submit that EN does not disclose or even suggest at least these features. Applicants acknowledge, for example, that Figs. 2G and 2H of EN show how a mask 160 is utilized to cover a nitride layer 150 above an NMOS device 102 while a second nitride layer 150 is removed from oxide layer 140 of the PMOS device 104. Applicants also acknowledge that EN discloses that the "resulting structure" shown in Fig. 2H creates "a tensile stress in the channel region 116 of the NMOS transistor 102" (see col. 7, 50-56). However, it is clear that this document does not specifically disclose or suggest removing, after the oxidizing step, oxide above the gate polysilicon of the n-type transistor. Applicants note, in particular, that col. 7, lines 36-39 of EN specifically indicates that "the oxide layer 140 serves as an etch-stop layer for the etch process ...". Thus, EN provides for removing the second nitride layer 150 and not the oxide layer 140 while the NMOS is masked. EN clearly does not disclose the removal of the oxide layer 140 from above the gate polysilicon of the n-type transistor.

Moreover, while the Examiner has alleged that EN discloses the formation, by an oxidizing step, of a bird's beak in an edge of the gate polysilicon, the Examiner has failed to identify any such structure in EN. The Examiner has failed to identify any such structure that is arranged within the channel of the n-type field effect transistor.

Applicants respectfully submit that independent claims 1 and 16 and claim 2, which depends from claim 1 are allowable. Accordingly, Applicants respectfully submit that the rejection under 35 U.S.C. § 102(e) should be withdrawn.

35 U.S.C. § 103 Rejections

Claims 1, 6-16, 21 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U. S. Patent No. 6,204,103 issued to BAI, *et al.* ("BAI") in view of EN. Claims 3-5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over EN in view of U. S. Patent No. 6,491,981 issued to CHANG, *et al.* ("CHANG"). These rejections are respectfully traversed.

In addition to the features noted above, claims 1 and 16 recite oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor. Claim 16 further recites that the oxidizing is performed without creating additional tensile stresses in a channel of the p-type field effect transistor. The oxidizing step results in formation of a bird's beak within the channel of the n-type field effect transistor in an edge of the gate polysilicon.

The Examiner has acknowledged on page 4 of the instant Office Action that BAI lacks any disclosure or suggestion with regard to "covering the p-type transistor with a mask and oxidizing a portion of the gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor without creating additional tensile stresses in a channel of the p-type transistor, and wherein the oxidizing step results in formation of a bird's beak in an edge of the gate polysilicon", and indicated that EN discloses these features. However, Applicants have clearly demonstrated above that EN also lacks a number of features recited in claims 1 and 16, and respectfully submit that no proper combination of BAI and EN disclose or suggest the combination of features recited in claims 1 and 16.

As noted above, while EN discloses how a mask 160 is utilized to cover a nitride layer 150 above an NMOS device 102 while a second nitride layer 150 is removed from oxide layer 140 of the PMOS device 104, and discloses that the "resulting structure" shown in Fig. 2H creates "a tensile stress in the channel region 116 of the NMOS transistor 102" (see col. 7, 50-56), EN does not does not specifically disclose or suggest removing, after the oxidizing step, oxide above the gate polysilicon of the n-type transistor. As noted above, col. 7, lines 36-39 of EN specifically indicates that "the oxide layer 140 serves as an etch-stop layer for the etch process ...". Thus, EN provides for removing the second nitride layer 150 and not the oxide layer 140 while the NMOS is masked. EN clearly does not disclose the removal of the oxide layer 140 from above the gate polysilicon of the n-type transistor. Moreover, while the Examiner has alleged that EN discloses the formation, by an oxidizing step, of a bird's beak in an edge of the gate polysilicon, the Examiner has failed to identify any such structure in EN. The Examiner has failed to identify any such structure that is arranged within the channel of the n-type field effect transistor.

Accordingly, Applicants submit that EN fails to cure the deficiencies of BAI which were clearly acknowledged by the Examiner to be missing from BAI.

With regard to CHANG, Applicants acknowledge that this document discloses a process of oxidizing a polysilicon layer 24a with a operating temperature from 550 to 750 degrees C. (see col. 3, lines 27-34). However, it is clear that CHANG fails to disclose or suggest any masking steps, much less, removing an oxide layer. It is also clear that CHANG lacks any disclosure with regard to creating a tensile stress in the channel of a n-type transistor. Finally, CHANG does not does not contain any

disclosure with regard to removing, after the oxidizing step, oxide above the gate polysilicon of a n-type transistor. Thus, CHANG also fails to cure the deficiencies of EN.

Applicants also submit that the dependent claims are distinguishable over the applied documents:

Claims 3-15, 21 and 22 are allowable over the cited references based on their dependencies from an allowable base claim. Additionally, claims 14 and 15 are further allowable based on their additional features.

Claims 14 and 15 recite that the step of oxidizing comprises oxidizing the gate polysilicon of the n-type field effect transistor to create a stress of about 700MPa in a channel of the n-type field effect transistor or about 500Pa to about 1000Pa. The Examiner maintains that the claimed tensile stress ranges lack criticality because Applicants do not teach that the tensile stress ranges solve any stated problem or are for any particular purpose. Applicants again respectfully traverse this submission, and direct the Examiner's attention to Figures 4 and 5, as well as to page 2 of the specification, where it is stated that tensile stresses in conventional n-type devices are relatively moderate (i.e., for example, about 200 MPa to about 300 MPa). Comparing the results of Figures 4 and 5 to these conventional results, it is seen that embodiments of the present invention offer improved tensile stress ranges, which are in embodiments are critical to their operation.

Additionally, Applicants further direct the Examiner's attention to page 10 of the specification, where it is noted:

> the oxidation of the gate of the NFETs creates large tensile stresses in the channel region of the NFETs ... Further, these tensile stresses increase electron mobility along the channel, and improve the performance of the NFETs.

At page 13, it is noted that the desired stresses are tensile and add values of the order of 200MPa and above. For these reasons, and because the cited references disclose a tensile stress of about 100 MPa, the tensile stress ranges recited in claims 14 and 15 are allowable. Consequently, allowance of claims 14 and 15 is respectfully requested.

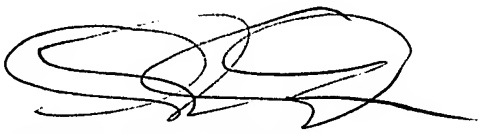
New Claims are also Allowable

Applicant submits that the new claims 24-25 are allowable over the applied art of record. Claims 24-25 recite a combination of features which are clearly not disclosed or suggested by the applied art of record. Specifically, Applicant submits that the applied documents fail to disclose or suggest, for example, depositing oxide on the gate polysilicon of the n-type transister, oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor, and removing the oxide above the gate polysilicon of the n-type transister, wherein the oxidizing step results in formation of a bird's beak in the channel of the gate polysilicon, as recited in claims 24 and 25. Accordingly, Applicants respectfully request consideration of these claims and further request that the above-noted claims be indicated as being allowable.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to **IBM Deposit Account No. 09-0458**.

Respectfully submitted,
Dureseti CHIDAMBARRAO, *et. al*



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